

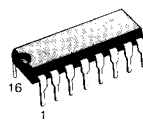
T54LS251
T74LS251



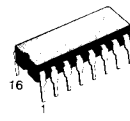
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The TTL/MSI T54LS251/T74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.



B1
Plastic Package



D1/D2
Ceramic Package



M1
Micro Package



C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS251 D2 T74LS251 C1
T74LS251 D1 T74LS251 M1
T74LS251 B1

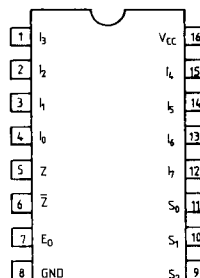
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

S_0 - S_2	Select Input
$\bar{E}_0$	Output Enable (Active LOW) Input
I_0 - I_7	Multiplexer Inputs
Z	Multiplexer Outputs
$\bar{Z}$	Complementary Multiplexer Output

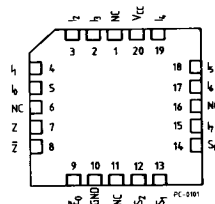
PIN CONNECTION (top view)

DUAL IN LINE



PC-0139

CHIP CARRIER

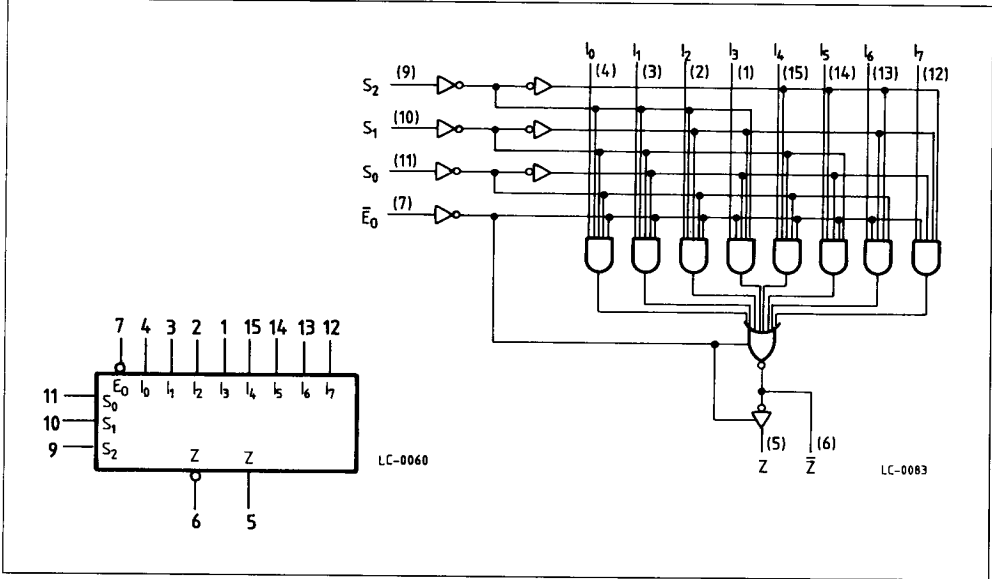


PC-0141

NC = No Internal Connection



LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	Input Voltage, Applied to Input	- 0.5 to 15	V
V _O	Output Voltage, Applied to Output	- 0.6 to 5.5	V
I _I	Input Current, Into Inputs	- 30 to 5	mA
I _O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS251D2	4.5 V	5.0 V	5.5 V	- 55°C to +125°C
T74LS251XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.



FUNCTIONAL DESCRIPTION

The LS251 is a logical implementation of a single pole, 8-position switch the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both as-

section and negation outputs are provided. The Output Enable input ($\bar{E}_0$) is active LOW. When it is activated, the logic function provided a the output is:

$$Z = \bar{E}_0 \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + \\ + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one, device

must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Outputs Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltage.

TRUTH TABLE

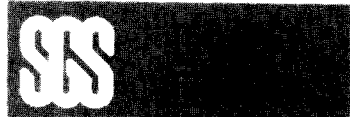
$\bar{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	L	L	X	X	L	X	X	X	X	X	H	L
L	L	L	L	X	X	H	X	X	X	X	X	L	H
L	L	L	H	X	X	X	L	X	X	X	X	H	L
L	L	L	H	X	X	X	H	X	X	X	X	L	H
L	L	H	L	X	X	X	X	L	X	X	X	H	L
L	L	H	L	X	X	X	X	H	X	X	X	L	H
L	L	H	L	X	X	X	X	X	L	X	X	H	L
L	L	H	H	X	X	X	X	X	X	X	X	L	H
L	L	H	H	X	X	X	X	X	X	H	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	L	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	L	H	X	X	X	X	X	X	H	X	H	L
L	H	H	L	X	X	X	X	X	X	X	L	L	H
L	H	H	L	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

(Z) = High Impedance (Off)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		$I_{OH} = -1.0\text{mA}$	V
		74	2.4	3.4		$I_{OH} = -2.6\text{mA}$	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	$I_{OL} = 4.0\text{mA}$	V
		74		0.35	0.5	$I_{OL} = 8.0\text{mA}$	
I_{OZH}	Output Off Current HIGH				20	$V_{CC} = \text{MAX}, V_{OUT} = 2.7\text{V}, V_E = 2.0\text{V}$	μA
I_{OZL}	Output Off Current LOW				-20	$V_{CC} = \text{MAX}, V_{OUT} = 0.4\text{V}, V_E = 2.0\text{V}$	μA
I_{IH}	Input HIGH Current			1.0	20 0.1	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$ $V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$	μA mA
I_{IL}	Input LOW Current				-0.4	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA
I_{OS}	Output Short Circuit Current (Note 2)		-20		-100	$V_{CC} = \text{MAX}, V_{OUT} = 0\text{V}$	mA
I_{CC}	Power Supply Current Outputs LOW Outputs Off			6.0	10	$V_{CC} = \text{MAX}, V_{OUT} = 4.5\text{V}, V_E = 0\text{V}$	mA
				7.0	12	$V_{CC} = \text{MAX}, V_{OUT} = 4.5\text{V}, V_E = 4.5\text{V}$	

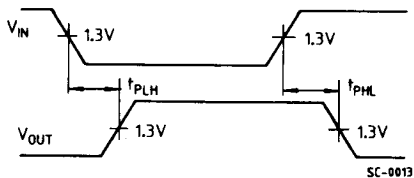
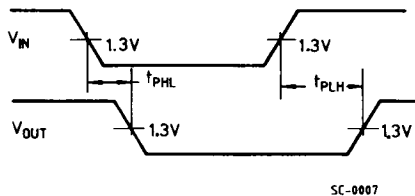
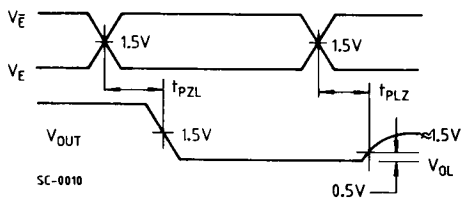
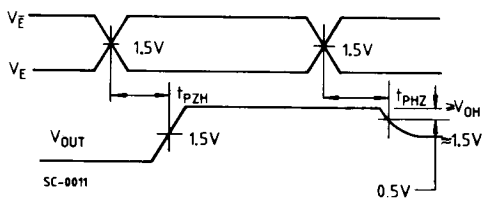
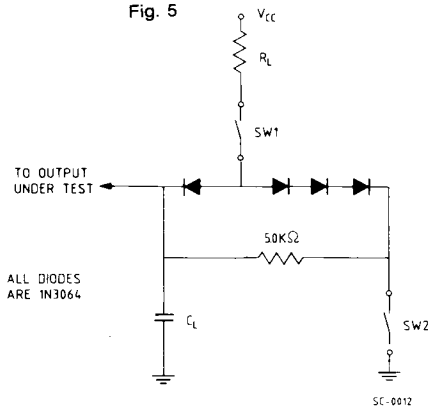
AC CHARACTERISTICS: ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH}	Propagation Delay, Select to Z Output		20	33	Fig. 1	ns
t_{PHL}	Propagation Delay, Select to Z Output		21	33	Fig. 2	
t_{PLH}	Propagation Delay, Data to Z Output		28	45	Fig. 1	
t_{PHL}	Propagation Delay, Data to Z Output		28	45	Fig. 1	
t_{PLH}	Propagation Delay, Data to Z Output		10	15	Fig. 1	
t_{PHL}	Propagation Delay, Data to Z Output		17	28	Fig. 1	
t_{PZH}	Output Enable Time to Z Output		17	27	Figs. 4,5	ns
t_{PZL}	Output Enable Time to Z Output		24	40	Figs. 4,5	
t_{PZH}	Output Enable Time to Z Output		30	45	Figs. 3,5	
t_{PZL}	Output Enable Time to Z Output		26	40	Figs. 3,5	
t_{PHZ}	Output Disable Time to Z Output		37	55	Figs. 3,5	
t_{PLZ}	Output Disable Time to Z Output		15	25	Figs. 3,5	
t_{PHZ}	Output Disable Time to Z Output		30	45	Figs. 4,5	ns
t_{PLZ}	Output Disable Time to Z Output		15	25	Figs. 4,5	

Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$

3-STATE AC WAVEFORMS AC LOAD CIRCUIT

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

SWITCHING POSITIONS

Symbol	SW1	SW2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pLZ}	Closed	Closed
t_{pHZ}	Closed	Closed